REMARKS

This paper is in response to the Office Action mailed on May 24, 2004.

Claims 26, 28, 29, 31, 32, 34, 38, 39, 40, 42, 43, 45, 47, 49, 50 are amended, claims 35-37 are canceled without prejudice or disclaimer, no claims are added; as a result, claims 26-34 and 38-52 are now pending in this application.

Claim 50 is amended to correct a typographical informality in the claim. Specifically, the claim was dependent on claim 1, which was previously canceled. The amendment clarifies the claim.

Applicant hereby incorporates by reference all prior responses to preserve issues for appeal. Applicant makes no admissions as to the substance or correctness of any rejection or qualification of any cited document as prior art.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§102 Rejection of the Claims

Claims 26, 29, 32, 35-39, 40, and 50-52 were rejected under 35 USC § 102(e) as being anticipated by Langendorf et al. (U.S. 6,505,282) or, in the alternative, under 35 USC § 103(a) Langendorf et al. (U.S. 6,505,282) in view of Margulis et al. (U.S. 5,392,239). Applicant respectfully traverses.

Claim 26 recites, in part, "a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode." Applicant is unable to find in Langendorf burst extended data out mode or a fast page mode. Applicant respectfully requests that the examiner specifically point to the location in Langendorf where a *fast* page mode is described. The Office Action points to Langendorf's abstract and Figs. 2-5 as showing a fast page mode. However, each of these locations discusses a page mode, not a fast page mode. As Langendorf does not teach all of the

features of claim 26, applicant submits that a *prima facie* case of anticipation or obviousness has not been made.

Claim 26 further recites, in part, "wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in Langendorf or in Margulis. As these documents do not teach all of the features of claim 26, applicant requests allowance of claim 26.

Claim 29 recites, in part, "wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in Langendorf or in Margulis. As these documents do not teach all of the features of claim 29, applicant requests allowance of claim 29.

Claim 32 recites, in part, , and wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or in Margulis. As these documents do not teach all of the features of claim 32, applicant requests allowance of claim 32.

Claims 35-37 are canceled without prejudice. Accordingly, the rejection thereof is now moot.

Claim 38 recites, in part, wherein the reading indicates an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or in Margulis.

As these documents do not teach all of the features of claim 38, applicant requests allowance of claim 38.

Claim 39 recites, in part, "wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, which indicates an extended data out mode for the first bank with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in Langendorf or in Margulis. As these documents do not teach all of the features of claim 39, applicant requests allowance of claim 39.

Claim 40 recites, in part, a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, wherein the data read indicates an extended data out mode when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or in Margulis. As these documents do not teach all of the features of claim 40, applicant requests allowance of claim 40.

Claims 50-52 depend at least in part on claim 49, which was not rejected as anticipated in view of Langendorf or Margulis, and are accordingly allowable therewith.

Alternatively, Claims 26, 29, 32, 35-39, and 40 were rejected under 35 USC 102(a) as being anticipated by Intel Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (INTEL) or , in the alternative, under 35 USC 103(a) Intel Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67,

11/96 (INTEL) further in view of Margulis et al. (U.S. 5,392,239). Applicant respectfully traverses.

Claim 26 recites, in part, "wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in any of the INTEL documents listed above or in Margulis. As these documents do not teach all of the features of claim 26, applicant requests allowance of claim 26.

Claim 29 recites, in part, "wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in any of the INTEL documents listed above or in Margulis. As these documents do not teach all of the features of claim 29, applicant requests allowance of claim 29.

Claim 32 recites, in part, , and wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in any of the INTEL documents listed above or in Margulis. As these documents do not teach all of the features of claim 32, applicant requests allowance of claim 32.

Claims 35-37 are canceled without prejudice. Accordingly, the rejection thereof is now moot.

Claim 38 recites, in part, wherein the reading indicates an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in any of the INTEL documents

listed above or in Margulis. As these documents do not teach all of the features of claim 38, applicant requests allowance of claim 38.

Claim 39 recites, in part, "wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, which indicates an extended data out mode for the first bank with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in any of the INTEL documents listed above or in Margulis. As these documents do not teach all of the features of claim 39, applicant requests allowance of claim 39.

Claim 40 recites, in part, a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, wherein the data read indicates an extended data out mode when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in any of the INTEL documents listed above or in Margulis. As these documents do not teach all of the features of claim 40, applicant requests allowance of claim 40.

§103 Rejection of the Claims

Claims 27-28, 30-31, 33-34, and 41-52 were rejected under 35 USC § 103(a) as being anticipated by Langendorf et al. (U.S. 6,505,282) or, in the alternative, under 35 USC 103 (a) Langendorf et al. (U.S. 6,505,282) in view of Margulis et al. (U.S. 5,392,239) and further in view of Suzuki et al. (U.S. 5,787,308). Applicant respectfully traverses.

Claim 27 depends from claim 26 and should be allowable with claim 26.

Claim 28 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or Margulis, either alone or in combination. As these documents do not teach all of the features of claim 28, applicant submits that claim 28 is allowable.

Claim 30 depends from claim 29 and should be allowable with claim 29.

Claim 31 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or Margulis, either alone or in combination. As these documents do not teach all of the features of claim 31, applicant submits that claim 31 is allowable.

Claim 33 depends from claim 32 and should be allowable with claim 32.

Claim 34 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or Margulis, either alone or in combination. As these documents do not teach all of the features of claim 34, applicant submits that claim 34 is allowable.

Claim 41 depends from claim 40 and should be allowable with claim 40.

Claim 42 recites, in part, a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller, wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, wherein the data read indicates an extended data out mode when the data read matches data written to the memory at address n using a known data pattern, and with the data

read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or Margulis, either alone or in combination. As these documents do not teach all of the features of claim 42, applicant submits that claim 42 is allowable.

Claim 43 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or Margulis, either alone or in combination. As these documents do not teach all of the features of claim 43, applicant submits that claim 43 is allowable.

Claim 44 depends from claim 43 and should be allowable with claim 43.

Claim 45 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements, wherein the data read indicates an extended data out set of requirements when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or Margulis, either alone or in combination. As these documents do not teach all of the features of claim 45, applicant submits that claim 45 and dependent claim 46 are allowable.

Claim 47 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes by indicating an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or Margulis, either alone or in combination. As these documents do not teach all of the features of claim 47, applicant submits that claim 47 and dependent claim 48 are allowable.

Claim 49 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements and to program the memory controller in accordance with the first and second sets of requirements by

indicating an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Langendorf or Margulis, either alone or in combination. As these documents do not teach all of the features of claim 49, applicant submits that claim 49 and dependent claims 50-52 are allowable.

Alternatively, claims 27-28, 30-31, 33-34, and 41-52 were rejected under 35 USC 103(a) as being anticipated by Intel Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (INTEL) or, in the alternative, under 35 USC 103(a) Intel Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (INTEL) further in view of Margulis et al. (U.S. 5,392,239) and further in view of Suzuki et al. (U.S. 5,787,308). Applicant respectfully traverses.

Claim 27 depends from claim 26 and is believed to be allowable as therewith as Suzuki does not cure the deficiencies of the INTEL documents and Margulis as references against the claims 26 and 27. Allowance of claim 27 is requested.

Claim 28 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in above listed INTEL documents, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 28, applicant submits that claim 28 is allowable.

Claim 31 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in above

listed INTEL documents, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 31, applicant submits that claim 31 is allowable.

Claim 34 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in above listed INTEL documents, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 34, applicant submits that claim 34 is allowable.

Claim 41 depends from claim 40 and should be allowable with claim 40.

Claim 42 recites, in part, a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller, wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, wherein the data read indicates an extended data out mode when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in above listed INTEL documents, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 42, applicant submits that claim 42 is allowable.

Claim 43 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in above listed INTEL documents, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 43, applicant submits that claim 43 is allowable.

Claim 44 depends from claim 43 and should be allowable with claim 43.

Claim 45 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements, wherein the data read indicates an extended data out set of requirements when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in above listed INTEL documents, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 45, applicant submits that claim 45 and dependent claim 46 are allowable.

Claim 47 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes by indicating an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in above listed INTEL documents, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 47, applicant submits that claim 47 and dependent claim 48 are allowable.

Claim 49 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements and to program the memory controller in accordance with the first and second sets of requirements by indicating an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in above listed INTEL documents, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 49, applicant submits that claim 49 and dependent claims 50-52 are allowable.

Claims 26, 29, 32, 35-39, and 50-52 were rejected under 35 USC 103(a) as being anticipated by Farrer et al. (U.S. 5,307,320) in view of Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 and further in view of Margulis et al. (U.S. 5,392,239). Applicant traverses.

Claim 26 recites, in part, "wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in Farrer, Micron Technical Note or Margulis. As these documents do not teach all of the features of claim 26, applicant requests allowance of claim 26.

Claim 29 recites, in part, "wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in Farrer, Micron Technical Note or Margulis. As these documents do not teach all of the features of claim 29, applicant requests allowance of claim 29.

Claim 32 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Farrer, Micron Technical Note or Margulis. As these documents do not teach all of the features of claim 32, applicant requests allowance of claim 32.

Claims 35-37 are canceled without prejudice. Accordingly, the rejection thereof is now moot.

Claim 38 recites, in part, wherein the reading indicates an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address

n+3 in a burst format. Applicant is unable to find these features in Farrer, Micron Technical Note or Margulis. As these documents do not teach all of the features of claim 38, applicant requests allowance of claim 38.

Claim 39 recites, in part, "wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, which indicates an extended data out mode for the first bank with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format." Applicant is unable to find these features in Farrer, Micron Technical Note or Margulis. As these documents do not teach all of the features of claim 39, applicant requests allowance of claim 39.

Claims 50-52 depend at least in part on claim 49, which was not rejected as obvious in view of Farrer, Micron Technical Note or Margulis, and are accordingly allowable therewith.

Claims 27-28, 30-31, 33-34, and 41-49 were rejected under 35 USC 103(a) as being anticipated by Farrer et al. (U.S. 5,307,320) in view of Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 and Margulis et al. (U.S. 5,392,239) and further in view Suzuki et al. (U.S. 5,787,308). Applicant traverses.

Claim 27 depends from claim 26 and is believed to be allowable as therewith as Suzuki does not cure the deficiencies of Farrer, Micron Technical Note, and Margulis as references against the claims 26 and 27. Allowance of claim 27 is requested.

Claim 28 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Farrer, Micron Technical

Note, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 28, applicant submits that claim 28 is allowable.

Claim 30 depends from claim 29 and should be allowable with claim 29.

Claim 33 depends from claim 32 and should be allowable with claim 32.

Claim 34 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features Farrer, Micron Technical Note, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 34, applicant submits that claim 34 is allowable.

Claim 41 depends from claim 40 and should be allowable with claim 40.

Claim 42 recites, in part, a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller, wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device, wherein the data read indicates an extended data out mode when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Farrer, Micron Technical Note, Margulis, or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 42, applicant submits that claim 42 is allowable.

Claim 43 recites, in part, wherein the processor is adapted to indicate an extended data out mode with data read from memory matching data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Farrer, Micron Technical Note, Margulis or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 43, applicant submits that claim 43 is allowable.

Claim 44 depends from claim 43 and should be allowable with claim 43.

Claim 45 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements, wherein the data read indicates an extended data out set of requirements when the data read matches data written to the memory at address n using a known data pattern, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Farrer, Micron Technical Note, Margulis or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 45, applicant submits that claim 45 and dependent claim 46 are allowable.

Claim 47 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes by indicating an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Farrer, Micron Technical Note, Margulis or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 47, applicant submits that claim 47 and dependent claim 48 are allowable.

Claim 49 recites, in part, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements and to program the memory controller in accordance with the first and second sets of requirements by indicating an extended data out mode with data read from memory matching data written to the memory at address n using a data pattern in a format selected from a group consisting of single discrete cycles and page mode cycles, and with the data read from memory matching the data written to the memory at address n+3 in a burst format. Applicant is unable to find these features in Farrer, Micron Technical Note, Margulis or Suzuki, either alone or in combination. As these documents do not teach all of the features of claim 49, applicant submits that claim 49 is allowable.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24th day of November, 2004.

Date 24 Nov '04 By

Timothy B Clise
Reg. No. 40,957